Limiting Factors of RF Performance Improvement as Down-scaling to 65-nm Node MOSFETs

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Abstract — As continuous down-scaling the RF MOSFETs into 65 nm node, the RF performance of $f_T$, $f_{\text{max}}$, and $NF_{\text{min}}$ also show the dependence on short channel effect owing to increasing drain current and transconductance. The device performance was improved by accurate higher drain bias conditions in the nano-scale devices, which produced a 20% enhancement of the saturation drain current, 5% $f_T$ increased and 3% lowered $NF_{\text{min}}$. The $NF_{\text{min}}$ of 0.63 dB, at 10 GHz under a drain bias of 1.2 V was found. However, the $f_T$ improves continuously to 65 nm node transistors, but the $f_{\text{max}}$ and $NF_{\text{min}}$ is limited at 65 nm node devices than 90 nm node devices due to the parasitic effect.

Index Terms — $NF_{\text{min}}$, $f_T$, $f_{\text{max}}$, MOSFET.

I. INTRODUCTION

The performance of Silicon radio frequency (RF) MOSFETs is improving so fast in the recent years, associated with the down-scaling of the Si technology [1]-[8]. The RF noise and high frequency gain can be improved significantly every generation. However, the bias condition is sensitive to device performance in nanometer generation [9]-[10]. The short channel effect related channel-length modulation and the non-saturation of drain current are the important concerns for the DC performance of highly scaled MOSFET. As continuous down-scaling the RF MOSFETs into 65 nm node, the RF performance of unity-gain cutoff frequency ($f_T$), maximum frequency of oscillation ($f_{\text{max}}$) and minimum noise figure ($NF_{\text{min}}$) still show much smaller dependence on short channel effect than DC drain current ($I_d$) and trans- conductance ($g_m$). However, although the $f_T$ improves continuously, the $f_{\text{max}}$ and $NF_{\text{min}}$ become worse at 65 nm node transistors than 90 nm node devices due to the limiting parasitic effect.

In this paper, we report the DC and RF performance of 65 nm node (45 nm physical gate length). Surprisingly, much smaller short channel effect on RF performance of $f_T$, $f_{\text{max}}$ and $NF_{\text{min}}$ were found than DC case. The non-saturating current is about ~20% variation when drain voltage is from 0.9V to 1.2V and also induces ~5.3% trans-conductance ($g_m$) variation for 65 nm RF MOSFETs.

In the meanwhile, the RF performance of cut-off frequency ($f_c$) increases 4.3% and minimum noise figure ($NF_{\text{min}}$) reduces 3% are also following the trans-conductance ($g_m$) variation. The major limiting factor of RF performance as scaling down to 65 nm node is the worse $f_{\text{max}}$ and $NF_{\text{min}}$ even though the $f_T$ is better due to the limiting parasitic effect.

II. EXPERIMENT DETAIL

Multiple gate-fingered 65nm node RF MOSFETs, with 45 nm physical gate length and SiN gate oxide with 30Å equivalent oxide thickness (EOT) were studied in this work. These were fabricated on a p-type Si substrate with its typical 10 $\Omega$-cm resistivity. The devices were fabricated on 12-in wafers at an IC foundry. To reduce the RF noise from the gate resistance and substrate network of their RF probing pads and the CPW lines, a microstrip line layout was used [1]-[3] instead of conventional CPW structure [4]-[7]. This was achieved by using Metal-1 (M1) as the ground plane of the transmission line [1]-[3], which allows direct measuring the $NF_{\text{min}}$ without complicated de-embedding. This is possible due to the shield of RF noise generated from the VLSI-standard low resistivity Si substrate [1]-[3]. Standard open- and through- test patterns were used in de-embedding the intrinsic S-parameters [11]-[13]. The devices were measured using an HP4155C, HP8510C and ATN-NP5B for DC I-V, S-parameters and $NF_{\text{min}}$, respectively. A device model with a BSIM core and parasitic RC elements to terminals was used to analyze the data [2],[7].

III. RESULT AND DISCUSSION

A. Short channel effect on RF performance:

Fig. 1 shows the $I_d$ - $V_d$ characteristics for a typical 65 nm node RF MOSFET. In saturation region ($V_{gs}$-$V_t$ < $V_d$), the $I_d$ and $g_m$ with different drain bias are discrepancy. An increase of 14.5% $I_{\text{d, saturation}}$ was observed as $V_d$ increased from...
0.9 to 1.2 V. The increasing of $I_{ds,sat}$ is imperative due to channel length modulation in nanometer devices. This also leads to a 6.8% increase of $g_m$ as shown in Fig. 2. Therefore, the DC characteristic with different drain bias in saturation region for short channel devices can not be neglected due to process variation or loading effect in circuit design.

![Fig. 1 The $I_d-V_d$ characteristics of 65 nm node RF MOSFETs for various $V_g$ biases.](image1)

![Fig. 2 The $I_d-V_g$ and $g_m-V_g$ characteristics of various $V_d$ biases for 65 nm node RF MOSFETs.](image2)

The RF current gain ($|H_{21}|^2$) and maximum available power gain ($G_{max}$) as a function of frequency for the 65 nm node devices is shown in Fig. 3(a). The unity-gain cut-off frequency ($f_T$) was obtained by the extrapolation of $|H_{21}|^2$ to 0 dB and $f_{max}$ by the extrapolation of $G_{max}$ to 0 dB. Similar to the DC case, the $|H_{21}|^2$, $G_{max}$, $f_T$ and $f_{max}$ also increased slightly as the drain bias increases from 0.9 to 1.2 V. This leads to the increase of the unity-gain cut-off frequency ($f_T$) from 162 GHz to 169 GHz. The lower current gain and $f_T$ at $V_d$ equal to 0.6 V is due to smaller drain current at non-saturation region. Figure 3(b) displays the $f_T$, $g_m$ and $|H_{21}|^2$ dependences for the 65 nm node RF MOSFETs. The $f_T$ curve follows the $g_m$ curve with respect to $V_{ds}$. Thus, the improvement in $f_T$ is consistent with the higher saturation current and higher $g_m$, arising from the channel-length modulation.

The RF noise is difficult to measure in Si MOSFETs due to the strong parasitic substrate loss that dominates the noise in as-measured $NF_{min}$. De-embedding is required to give the much smaller intrinsic $NF_{min}$ but it can produce errors. Our transmission line layout permitted the direct measurement of the intrinsic $NF_{min}$, without the need for de-embedding of the parasitic pads and the substrate loss [1]-[3]. Fig. 4 displays the as-measured $NF_{min}$ as a function of frequency. The low $NF_{min}$ of 0.63 dB at 10 GHz under a drain bias of 1.2 V was obtained for 65 nm node RF MOSFETs. The measured $NF_{min}$ shows a similar improving trend with increasing $V_{ds}$ also shown in Fig. 3(b). At 10 GHz, $NF_{min}$ values of 0.68, 0.65, 0.64 and 0.63 dB were obtained for $V_d = 0.6, 0.9, 1.0$ and 1.2 V. It is worth noting that the improved noise is important when short-channel devices are operated at RF frequencies.

![Fig. 3 (a) The $|H_{21}|^2$ and $G_{max}$ vs. frequency of various $V_d$. (b) The cut-off frequency ($f_T$), $g_m$ and $NF_{min}$ vs. $V_d$ bias.](image3)
Fig. 4 The $NF_{\text{min}}$ of various $V_d$ biases for 65 nm node RF MOSFETs. The line is simulation data.

Table 1 summarizes the DC & RF device parameters for 65 nm MOSFETs at different $V_d$. The amount of variation to drain bias is much lower for RF $f_T$, $|H_21|^2$, $G_{\text{max}}$ and $NF_{\text{min}}$ than DC $I_{\text{dsat}}$ and $g_m$ suffering from short channel effect. The lower variation of $f_T$ is due to the increasing feedback and parasitic capacitance at higher $V_d$ that compensates the $g_m$ increase in following equation:

$$f_T = \frac{g_m}{(C_{gs} + C_{gd})}$$

The smaller $NF_{\text{min}}$ variation is due to the dominating gate resistance ($R_g$) and $g_m$ product in square root in combination of the smaller $f_T$ variation from a circuit-theory-derived equation [7]:

$$NF_{\text{min}} = 1 + 2 \frac{f_T}{f_T} \sqrt{(\gamma + \frac{4}{15})(\gamma + g_m R_g)}$$  (2).

Here $\gamma$ is the drain current noise correlation factor – where the ideal value of 2/3 was used in the fitting procedure. Good agreement between the measured and eq. (2) calculated $NF_{\text{min}}$ are also shown in Fig. 4. From eq. (2) one can deduce that the primary factor leading to the moderate improvement in $NF_{\text{min}}$ at higher $V_d$ is the increase in $f_T$.

**B. Degraded $f_\text{max}$ & $NF_{\text{min}}$ under improved $f_T$ during scaling:**

Figs. 5 and 6 show the down-scaling trend of the $f_T$, $f_\text{max}$, $NF_{\text{min}}$, $g_m$ and $R_g$ characteristics from LG of 0.18 μm to 65 nm, where the data of 90 to 0.18 μm node devices are from earlier reports [1]-[3], [8]. The $NF_{\text{min}}$ and $f_\text{max}$ shows degraded performance as scaling to 65 nm node devices even though having the higher $f_T$. The degraded $NF_{\text{min}}$ on the down-scaled LG is due to the higher $R_g \times g_m$ by the eq. (2). For 90 nm to 0.18 μm node devices, the $NF_{\text{min}}$ decreases with gate length due to small $R_g$ and $g_m$ makes the $R_g \times g_m$ less significant than $\gamma$- the drain current noise correlation factor. However, both the better $g_m$ and poorer $R_g$ dominate the $NF_{\text{min}}$ at 65 nm node devices. The higher $R_g$ is unavoidable due to shorter LG at highly scaled transistors, which also causes the degradation of $f_\text{max}$ even though under the higher $f_T$ during scaling:

$$f_\text{max} = \frac{f_T}{2\sqrt{(R_g + R_g + R_g)g_{ds} + 2\pi f_T R_g C_{gd}}}$$  (3).

Therefore, the degradation of $R_g$ largely limits the further improvement of $f_\text{max}$ and $NF_{\text{min}}$ at sub-65 nm node devices due to the limiting parasitic effect. Further improving the RF performance for 65 nm node devices or below is using the CMP-planar process to replace the gate and gate electrode materials as recently developed [14].

Fig. 5 Measured $f_T$, $f_\text{max}$ and $NF_{\text{min}}$ of down-scaled RF MOSFETs.

<table>
<thead>
<tr>
<th>Device @ $g_{m,\text{max}}$ ($V_g$=1.0V)</th>
<th>$V_d$=0.9V</th>
<th>$V_d$=1.0V</th>
<th>$V_d$=1.2V</th>
<th>% (from 0.9 to 1.2V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation current $I_{\text{dsat}}$ (mA)</td>
<td>20</td>
<td>21</td>
<td>22.9</td>
<td>14.5</td>
</tr>
<tr>
<td>Transconductance $g_m$ (mS)</td>
<td>41.1</td>
<td>42.6</td>
<td>43.9</td>
<td>6.8</td>
</tr>
<tr>
<td>Gate resistance $R_g$ (Ω)</td>
<td>28</td>
<td>28</td>
<td>28</td>
<td>-</td>
</tr>
<tr>
<td>Cut-off frequency $f_T$ (GHz)</td>
<td>162</td>
<td>166</td>
<td>169</td>
<td>4.3</td>
</tr>
<tr>
<td>Current gain $</td>
<td>H_21</td>
<td>^2$ (dB)</td>
<td>42.6</td>
<td>42.9</td>
</tr>
<tr>
<td>Max. power gain $G_{\text{max}}$ (dB)</td>
<td>26.1</td>
<td>26.2</td>
<td>26.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Min. noise figure $NF_{\text{min}}$ (dB)</td>
<td>0.65</td>
<td>0.64</td>
<td>0.63</td>
<td>3.2</td>
</tr>
</tbody>
</table>
Fig. 6 Measured $g_{m}$ and $R_{g}$ of down-scaled RF MOSFETs.

IV. CONCLUSIONS

We have shown the RF performance can be improved at accurate drain bias for 65 nm node MOSFETs. Typical values for $NF_{min}$ were 0.63 dB at 10 GHz and 169 GHz for $f_{t}$ of 65nm RF MOSFETs. In spite of the strong dependence of short channel effect on DC characteristics at 65 nm node devices, the RF performance is limited by the parasitic effect that requires novel device and process optimization.

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