A 0.18 μm CMOS UWB LNA with New Feedback Configuration for Optimization Low Noise, High Gain and Small Area

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Abstract - In this paper, we present the low noise amplifier using new feedback connection configurations. The UWB LNA is design in 0.18 μm TSMC CMOS technique to achieve high gain, small size and low noise. The LNA achieved 11 dB of average power gain, low 2.87 dB noise figure (NF), -10.9 dB input match, -7 dB return loss, -3 dBm of IIP3 and only 0.54 mm² size with 15 mW power consumption.

Index Terms—Feedback, Low noise amplifier, low power.

I. INTRODUCTION

Ultra-wideband technology using the unlicensed frequency band from 3.1 to 10.6 GHz has become much interest of broadband wireless communication due to its high data rates, low power transmission, robustness for multi-path fading and low power dissipation. Among possible applications, UWB technology may be used for imaging systems, vehicular and ground penetrating radars, Radio-frequency identification (RFID) and communication systems. The basic requirement in the UWB transceiver is a wideband low noise amplifier (LNA). It must provide good input impedance matching, low power consumption, low noise performance, and sufficient gain with good S/N for the following stages, and small size over the entire frequency band [1]-[18]. Recently, the CMOS technology is an attractive solution for UWB LNA system due to its mature technologies, low cost, high level integration with baseband digital circuits for System-on-Chip (SoC) and even high performance for down-scaling devices in terms of cut-off frequency [19]-[20] and inductor Q-factors [21]-[22]. Several different approaches have been proposed to establish a universal standard for such applications [7]-[18]. The feedback configuration is one of the suggestion topologies to build a wideband and low noise for RF transceiver front-end [10]-[15].

In this work an ultra-wideband CMOS LNA is proposed using new RC-feedback connection and LC shunt topology, implemented in 0.18 μm CMOS technology. The new RC-feedback connection configuration can achieve wideband input matching, good linearity [10]-[12] and low noise. The LC shunt topology can rise up high frequency gain and extent to wide bandwidth. Therefore, the UWB LNA achieved a 11 dB average power gain, a 2.87 dB NF, input reflect loss less than -10.9 dB, output return loss less than -7 dB and the input IIP3 is -3 dBm from ultra-wide band LNA circuit. These results are suitable for UWB LNA circuit application.

II. CIRCUIT DESIGN

The UWB LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption. The LNA also needs to have a good input mating over the whole band to capture the transmitted RF energy efficiently. Figure 1 shows a schematic of the proposed three-stage amplifier. The first stage is the RC-feedback cascode topology that provides high gain, wider bandwidth, better stability and well reverse isolation. The middle stage is an inductor-capacitor parallel configuration (Lᵣ/Cᵣ) to pull up high frequency gain. The output stage is a simple current buffer that gives broadband out impedance of 50 Ω for measurement purposes.

Fig. 1. Schematic of the ADS-designed UWB CMOS shunt resistive-feedback LNA circuit which uses TSMC’s 0.18μm RF CMOS technology. The dashed circle is Lᵣ/Cᵣ shunt topology.
A. Input and output Matching:

For input matching, we used RC-feedback cascode topology for matching. The cascode configuration can reduce the high frequency roll-off of the input devices due to the Miller effect to provide input and output matching independently. We can select $R_f$ and $C_f$ components to achieve good input matching and high gain.

The output stage is used current buffer, $M_3$ is the source follower and the $M_4$ provide the stable current source for $M_3$, to tune the whole frequency to achieve $50 \Omega$. The output impedance is derived as:

$$Z_{out} = \frac{1}{g_{m3}||r_{o4}} = \frac{1}{g_{m3}}. \quad (1)$$

We only fine tune the bias and transistors size to achieve good output matching.

B. Wideband Design:

The RC-feedback loop is one of the most popular to use in amplifiers circuit for its wideband input matching and good linearity. The substrate bias of transistor $M_1$ is used to raise the gain and reduce the power dissipation. However, the gain is confined at high frequency due to gate-drain capacitance and gate-source capacitance. For further rise up the gain at higher frequency, the $L_{by}/C_{by}$ configuration is connected to the second stages to extend bandwidth as the dashed circle in Fig. 1. The $L_{by}/C_{by}$ is chosen to resonate at 10.6GHz for the bandwidth extension. The power gain ($S_{21}$) can increase about 7.13 dB at 10.6 GHz as shown in Fig. 2. The wide band and high gain is obtained in feedback LNA circuit design.

\[ \text{Fig. 2. Simulated power gain (S}_{21}\text{) with and without L}_{by}/C_{by} \text{ parallel topology.} \]

C. Minimizing NF:

The noise figure is dominated of the first stage for the multi-stages amplifier due to the $NF_{tot}$ is derived from $[2]$:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{\text{pl}}} + \cdots + \frac{NF_{n} - 1}{A_{\text{pl}} \cdots A_{\text{pl}(n-1)}}. \quad (2)$$

The first stage of the receiver system is LNA. Therefore, reducing the noise figure is important for LNA design.

For minimizing the NF of UWB LNA, the new RC-feedback connection topology is used. The RC-feedback topology in first stage is dominated the noise characteristics for LNA. Compare with general circuits [11]-[16], the proposed RC-feedback topology is connected in front of the matching gate inductor ($L_g$). The feedback noise current ($i_f$) do not pass through the parasitic resistance of gate inductor ($R_{ds}$). Therefore, the noise figure can be reduced using new feedback topology circuit. Fig. 3 shows the NF comparison with general feedback topology and new feedback connection. At 10.6 GHz the NF can be lower ~0.54 dB of new feedback connection than general feedback topology. A high voltage and low noise UWB LNA can be achieved. The observation of our design is presented in the following section.

\[ \text{Fig. 3. Simulated noise figure (NF}_{min}\text{) using general circuit and new feedback connection to compare.} \]

III. SIMULATION RESULTS

The CMOS UWB LNA was simulated using Advance Design System (ADS) software. The layout plays an important role for RF circuit performance due to the lossy Si substrate. Therefore, the EM simulation to optimize the UWB LNA performance is needed for circuit design. The parameters of EM simulation is using TSMC CMOS 0.18 $\mu$m technology with 1.8 supply voltage.

Figures 4 and 5 show the two-port EM simulated S-parameters from 1 GHz to 16 GHz. Figure 5 shows the dependence of simulated input reflection coefficient ($S_{11}$) and output return loss ($S_{22}$) on frequency. The simulated $S_{11}$ is lower than -10.9 dB for input matching across the frequency band of 3.1~10.6 GHz. The simulated $S_{22}$ is less than -7 dB for output matching over a 3.1~10.6 GHz range. In Figure 6 the simulated forward gains ($S_{21}$) and reverse isolation ($S_{12}$) are reported for the UWB LNA circuit. The $S_{21}$ displays a maximum gain of 13.1 dB at 3.1 GHz and the average $S_{21}$ value over the 3.1-10.6 GHz frequency band is 11 dB. With
RC-feedback topology, the bandwidth extends to cover from 3.1 to 10.6 GHz. An excellent $S_{12}$ of less than -27 dB is obtained due to effective cascode configuration. It is noted that the input impedance is optimized for low noise figure while keeping the corresponding return loss at an acceptable level.

To optimize the performance, the transistors have been sized to provide good noise characteristics, while allowing a good input impedance matching over the required bandwidth. The simulated NF of the implemented amplifier is shown in Figure 7. The simulated NF shows a minimum value of 2.87 dB at 7.5 GHz. The simulated NF range was 2.87~3.67 dB over the 3.1~10.6 GHz range. Figure 8 shows the two-tone test for third-order intermodulation distortion of the UWB CMOS LNA circuit. The third order input intercept point (IIP3) is -3 dBm.

Figure 8 shows the layout of the UWB LNA using new feedback connection. We only used three inductors, four transistors, two capacitors, and four resistors to constitute the LNA. The total occupied chip size of the CMOS UWB LNA including the probe pads is 0.727 mm × 0.744 mm and the power consumption is 15.01 mW with taking into account the output buffer stage.
Table 1 summarizes the measured performance of the LNA and compares the other reported circuit performance. Our proposed CMOS LNA can achieve a wide bandwidth, high gain, good linearity, very low NF and low power consumption, and compares well with other published reports [14]-[16].

Table 1. Comparison of LNA circuit performance: published and this work.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>[14]</th>
<th>[15]</th>
<th>[16]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW (GHz)</td>
<td>2.8±2.7</td>
<td>3.1±10.6</td>
<td>1.2±11.9</td>
<td>3.1±10.6</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>&lt; -4</td>
<td>&lt; -9.7</td>
<td>&lt; -11</td>
<td>&lt; -10.9</td>
</tr>
<tr>
<td>S22 (dB)</td>
<td>&lt; -7.5</td>
<td>N/A</td>
<td>N/A</td>
<td>&lt; -7</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>16±19.5</td>
<td>7.4±9.2</td>
<td>5±9.7</td>
<td>8.9±13.1</td>
</tr>
<tr>
<td>NFmin (dB)</td>
<td>3.1±3.8</td>
<td>4.1±7</td>
<td>4.2±5.1</td>
<td>2.87</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-1</td>
<td>7.25</td>
<td>-6.2</td>
<td>-3</td>
</tr>
<tr>
<td>PD (mW)</td>
<td>32</td>
<td>23.5</td>
<td>20</td>
<td>15.01</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>1.63</td>
<td>0.78</td>
<td>0.59</td>
<td>0.54</td>
</tr>
<tr>
<td>Topology</td>
<td>0.18 μm Feedback</td>
<td>0.18 μm Feedback</td>
<td>0.18 μm Noise-Canceling</td>
<td>0.18 μm Feedback</td>
</tr>
</tbody>
</table>

IV Conclusion

A CMOS UWB LNA with new feedback connection configuration has been designed. This UWB LNA exhibited a high 13.1 dB gain, low 2.87 dB NF, input reflect loss less than -10.9 dB, output return loss less than -7 dB and the input IIP3 is -3 dBm from 3.1 to 10.6 GHz, while only 15 mW power dissipation. The proposed LNA satisfies UWB LNA system requirements.

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REFERENCES