A Novel Compact Complementary Colpitts Differential CMOS VCO with Low Phase-Noise Performance

Chien-Cheng Wei, Hsien-Chin Chiu, Yi-Tzu Yang, and Wu-Shiung Feng

Department of Electronic Engineering, Chang Gung University, Taoyuan, Taiwan, Republic of China

Abstract — A low phase-noise Ka-band CMOS voltage-controlled oscillator is proposed in this paper. The CMOS VCO core adopts a new complementary Colpitts structure in a 0.18-μm CMOS technology to achieve the differential-ended outputs with low phase-noise performance, as well as operate at much higher frequency. The VCO oscillates from 29.8 to 30 GHz with 200MHz tuning range. The measured phase-noise at 1-MHz offset is -109 dBc/Hz at 30 GHz and 105.5 dBc/Hz at 29.8 GHz. The power consumption of the VCO core is only 27 mW. To the authors’ knowledge, the proposed CMOS VCO achieves the best figure of merit (FOM) of -185 dB at 29.95-GHz band.

Index Terms — Voltage-controlled oscillators (VCOs), low phase-noise, complementary Colpitts, differential-ended.

I. INTRODUCTION

Recently, with advances in radio frequency (RF) CMOS technology, CMOS technology has been extensively adopted in wireless communication applications because of their low cost and the ability to be integrated with digital circuits. However, owing to the increase in the operation frequency in the modern communication systems, a high-quality voltage-controlled oscillator (VCO) in RF transceiver is quite demanded to generate local clocks for mixing the RF and IF signals. Therefore, design and implementation of low phase-noise CMOS VCOs is known as a big challenging block due to the inborn limitations of standard CMOS process technology. Most of the previously studies describe some high-performance VCOs in cross-coupled topologies [1]–[5] by using their proposed techniques. In these techniques, the layout issues such as active and passive devices design were major discussed to optimize the phase-noise performance. And the reduction in the parasitics effects was also analyzed to overcome the drawbacks that could be easily appeared in the higher frequency-bands.

Therefore, in order to provide a high-quality LO signal in millimeter wave regions, a new complementary Colpitts oscillator is introduced in this paper. The novel topology is simply constructed of two transistors and a passive LC network. A complementary PMOS and NMOS transistor pair was employed to generate a larger negative-resistance, and a center-tapped inductor with grounded capacitors were used to form the resonate tank and balance the phase and amplitude of two outputs. Besides, this topology requires no additional bias circuit for VCO core and buffer interfaces. Thus, compared to the other topologies oscillated at around 30 GHz, the novel complementary Colpitts VCO with differential-ended outputs achieves larger transconductance, lower phase-noise, and more relaxed oscillation condition within an uncomplicated structure and small size.

II. VCO DESIGN AND IMPLEMENTION

The most popular oscillator in modern CMOS circuits is the LC tank cross-coupled oscillator. In general, the complementary structure shows a better performance than the NMOS-only and PMOS-only structure, as a result of the reduced hot carrier effect, better up/down swing symmetry, and higher transconductance of the constituting transistors [3]. However, the Colpitts oscillator is also a well-known topology of the oscillators. Compared to the above common cross-coupled oscillators, the Colpitts oscillator provides the better performance in phase-noise owing to its highest power-transferred efficiency [7]. Therefore, a previous study proposed a new architecture of combining the complementary and Colpitts oscillator [4], as depicted in the Fig. 1(a). A common-source configuration with one inductor and two capacitors were introduced to form the Colpitts structure. The PMOS M2 stacked on the top of NMOS M1, was employed to replace the large-size inductor as a RF choke, as well as increase the overall transconductance for larger negative-resistance.

Fig. 1 (a) Published complementary Colpitts oscillator in [4]. (b) Proposed new complementary Colpitts oscillator topology.
However, the proposed complementary Colpitts oscillator in [4] only operates for single-ended output, which cannot be applied in differential-ended systems owing to the unbalance output power and phase between $V_d$ and $V_g$. Therefore, a novel LC network is introduced in the complementary Colpitts oscillator core to generate a 180° out of phase between gate and drain terminals of $M_1$ and $M_2$, as shown in Fig. 1(b). The proposed LC network is composed of two series inductors $L_1$ and $L_2$ with three grounded capacitors $C_1$, $C_2$, and $C_T$. The grounded capacitor $C_T$ is an important key parameter to adjust the phase and amplitudes between two output ports. From the small-signal analysis, the transfer function between gate terminal ($V_g$) and drain terminal ($V_d$) in Fig. 1(b) can be expressed as

$$V_d = -V_g \left(1 - \omega^2 L_1 C_1 + \omega^2 L_2 C_1 + \omega^2 C_l L_2 - \omega^2 L_1 C_1 C_T \right)$$

(1)

And after deriving the close-loop of the proposed circuit, the oscillation frequency can be approximated by

$$\omega_0 \approx \sqrt{\frac{C_1 + C_T + C_2}{L_1 L_2 C_1 C_2 C_T}}$$

(2)

Assuming that the two inductance $L_1$ and $L_2$ in (1) are identical owing to the use of center-tapped inductor in this design, the two terms of $\omega^2 L_1 C_1$ and $\omega^2 L_2 C_2$ in (1) can be neglected at first. And then substituting the oscillation frequency $\omega_0$ of (2) into (1), the relationship between two outputs can be found that $V_g \approx -V_d$, which means the amplitudes of two outputs are approximately the same with a phase difference of 180°. Fig. 2 displays the simulated results of output waveforms at gate and drain terminals, respectively. And the simulated results of $C_T$ value versus the difference of output power and phase is shown in Fig. 3. These results show that the proposed LC network can optimize the output waveforms after carefully choosing the value of $C_T$.

Thus, by adopting the low-parasitic and high-transconductance topology, there exists more potential in the design of a low-noise oscillator in high frequency with low power. Traditionally, the Colpitts oscillator is a simple oscillator core, which has been the most favored topology for low phase-noise [6-8]. However, since the conventional Colpitts oscillator needs additional circuits for bias and buffer interfaces, its oscillation performances may be degraded by the parasitics in high frequency. In this work, the novel complementary Colpitts adopts the self-bias technique for VCO core and buffer interface, which provides better oscillation performance compared to other topologies. Fig. 4 plots the fully circuit schematic of the proposed complementary Colpitts differential CMOS VCO. The grounded capacitors $C_1$ and $C_2$ were replaced by the accumulation-mode varactors as the control component for fine-tuning the oscillation frequency. Besides, in order to drive the 50-Ω load of test instrument, the open-source buffers and the external bias-tees were employed.
III. Measurement Results

By using a 0.18-μm CMOS 1P6M standard process from Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), a 30 GHz new complementary Colpitts VCO with differential outputs was implemented for demonstration. To characterize the circuit performance of the proposed VCO, the on-wafer measurement was utilized in this work. Fig. 5 shows the microphotograph of the fabricated circuit, a symmetrical layout is used for VCO design to ensure the fully differential operation. The total chip area including the dc and rf pads is 0.6 × 0.4 mm², where the active area occupy only around 0.45 × 0.3 mm². The designed VCO including two output buffers operates at a supply voltage of 1.8 V with total power consumption of 27 mW. Fig. 6 plots the oscillation frequencies were from 29.8 to 30 GHz under controlled voltages from –0.6 to 1.5 V. This figure also shows the measured output spectrum at controlled voltages of 0.5 V, which demonstrates that the proposed VCO structure can easily work at millimeter wave frequency band owing to its lower parasitic. Fig. 7 and 8 plots the measured output power and its related close-in phase-noise by using the Agilent E4407B spectrum analyzer and E5052A signal source analyzer, respectively. And all losses from the adaptors, cables, and bias-tees in the measurement setup were calibrated and deembedded in the experimental results. As shown in Fig. 7, the measured output power of the differential ports, gate port and drain port, were both higher than –7 dBm and have a similar power level. It is because the new complementary Colpitts VCO adopted a proposed LC network to balance the output power between the two ports. The measured phase-noise, as shown in Fig. 8, was 110 dBc/Hz at 1 MHz offset at oscillated frequency of 29.95 GHz. The above measurement of free-running phase-noise shows that the Ka-band CMOS VCO is sufficient for wireless communication applications. However, by utilizing the VCO in a 30 GHz frequency synthesizer, the phase-noise can be further suppressed by the loop filter of the frequency synthesizer. Table I compares the Ka-band VCOs released over the past few years. It shows that the phase-noise of this novel VCO is the lowest of any circuit operated near 30 GHz. The figure-of-merit (FOM) is also the best record of –185dBc/Hz compared to other applications.

![Microphotograph of the fabricated VCO.](image)

**TABLE I**

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Year</th>
<th>Process</th>
<th>$P_{DC}$</th>
<th>$f_0$</th>
<th>Phase noise</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>2004</td>
<td>0.12μm HBT</td>
<td>3.7mW</td>
<td>33GHz</td>
<td>-99dBc/Hz 1MHz offset</td>
<td>-183dBc/Hz</td>
</tr>
<tr>
<td>[10]</td>
<td>2003</td>
<td>0.15μm pHEMT</td>
<td>80mW</td>
<td>28.3GHz</td>
<td>-102dBc/Hz 1MHz offset</td>
<td>-172dBc/Hz</td>
</tr>
<tr>
<td>[11]</td>
<td>2006</td>
<td>0.35μm CMOS</td>
<td>117mW</td>
<td>30.9GHz</td>
<td>-102dBc/Hz 1MHz offset</td>
<td>-171dBc/Hz</td>
</tr>
<tr>
<td>This work</td>
<td>2007</td>
<td>0.18μm CMOS</td>
<td>27mW</td>
<td>29.9GHz</td>
<td>-110dBc/Hz 1MHz offset</td>
<td>-185dBc/Hz</td>
</tr>
</tbody>
</table>

![Performance of the oscillation frequency and the measured output spectrum for the proposed VCO.](image)
VII. CONCLUSION

In this paper, we demonstrated a Ka-band CMOS VCO based on a new complementary Colpitts topology in 0.18-μm CMOS technology. The VCO operates from 29.8 to 30 GHz with 0.6% tuning range, and provides a good phase-noise of -110 dBc/Hz at 1 MHz offset. By adopting the proposed LC network, the VCO can work at differential operation. Compare with the other VCOs oscillated at near 30 GHz, the novel VCO exhibits the best record of FOM of -185 dBc/Hz at 29.95 GHz band.

ACKNOWLEDGEMENT

The authors would like to acknowledge fabrication support provided by Taiwan Semiconductor Manufacturing Company (TSMC) through the National Chip Implementation Center (CIC).

REFERENCES