A Ka-Band Monolithic CPW-Mode T/R Modules Using 0.15 μm Gate-Length GaAs pHEMT Technology

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Abstract — This paper presents the designs and measurement results of the monolithic coplanar waveguide (CPW) Ka-band millimeter wave integrated circuits, including low noise amplifier, single-balance mixer, power amplifier, and oscillator. The millimeter wave ICs were fabricated with a 0.15 μm T-shape gate GaAs pseudomorphic HEMTs technology, carried out by commercially available foundry. The CPW process was applied in this work to avoid backside process and various impedances can also be adjusted by line width and gap. Therefore, these sub-circuits can be integrated using CPW technology easily and no via-hole process was involved to reduce the process cost.

Index Terms — Millimeter wave, GaAs pHEMT, CPW, amplifier, oscillator, mixer.

I. INTRODUCTION

GaAs-based pseudomorphic high electron mobility transistors (pHEMTs) have emerged as one of the most important technologies for a variety of advanced microwave and millimeter wave systems. As the wireless communications become more and more popular, the application frequency is moving toward higher frequency range such as K-band (18-27 GHz), Ka-band (28-35GHz), or above due to the bandwidth crowd blow 10 GHz. For past decades, sub-micron GaAs pHEMT was used for multifunctional applications such as high power, high efficiency, and low noise up to W-band. Because of its broad applicability to a multitude of system requirements, low cost pHEMT manufacturing urgently needs to be developed to cope with this increasing demand at millimeter wave. However, high cost of this industry also limited its development to commercial applications and was difficult to extend its market. In this regard, we implemented the millimeter wave low noise amplifier (LNA), single-balance mixer, power amplifier (PA), and oscillator using coplanar waveguide architecture. CPW microstrip line was used for millimeter circuit passive components and interconnection. Compared to conventional via-hole process in standard GaAs foundry, foundry deliver time and cost can be reduced simultaneously. The sub-circuits of Ka-band transceiver/receiver (T/R) were implemented using WIN Semiconductors standard PP15-20 process line. Based on the measured results in this study, The Ka-band T/R modules really exhibit highly potential for low cost millimeter wave circuit applications.

II. APPROACH

Three key points were optimized to achieve the results presented in this work: 1) The uniformity of 0.15 μm gate length GaAs pHEMT 2) The CPW simulation environment establishment and its relation to measurement results 3) Sub-circuits simulation accuracy correspond to measurement results.

A. pHEMT Process Optimization

Figure 1 shows the SEM cross-sectional microphotograph of 0.15 μm gate length GaAs pHEMT. For device fabrication, excluding gate lithography, others patterns were processed by optical stepper lithography and lift-off technology. Ohmic contacts were realized by using Au/Ge/Ni/Au alloy followed by a 430°C, 15 seconds rapid thermal annealing (RTA) alloy. Ion-implant isolation technology was used for mesa isolation to prevent the flow of any side-wall gate leakage current. After the highly selective citric acid chemical gate recess process, 0.15μm-long Ti/Pt/Au-gates were direct written by e-beam writer and were deposited by lift-off process. Then, a 1500 Å SiNₓ was deposited by plasma enhance chemical vapor deposition (PECVD) at 280 °C for passivation. For the interconnection above the passivation layer, we
applied 2 μm Au to minimize the series resistance and to obtain a high stability to moisture. The current gain cutoff frequency \(f_T\) and maximum oscillation frequency \(f_{\text{max}}\) were 98 GHz and 150 GHz, respectively. Nevertheless, the run-to-run variation of \(f_T\) and \(f_{\text{max}}\) were less than 5%. The device were also pass 85-85 (temperature = 85 °C, humidity = 85%) reliability evaluation at \(V_{ds}\) of 3V more than 3000 hours.

B. CPW MICROSTRIP LINE

Figure 2 depicts the die photograph of a coplanar T-junction with a shorted stub connected at the third port and its related equivalent circuit model. The characteristic impedance was designed at 50Ω for minimizing the transition loss (Line Width = 10μm and gap between signal line and ground is 5μm). Figure 3 shows the measured and simulated results of T-junction return loss, and its insertion loss results were less than 0.5 dB at 30GHz. Based on the measured results, they show a good agreement between the EM simulation and measurement results of return and insertion losses in the Ka-band region.

C. CIRCUITS DESIGN AND MEASUREMENT

The CPW technology was used for Ka-band circuits design, which were fabricated by WIN 0.15 μm GaAs pHEMT with 6-inch wafers thinned to 100-μm. As shown in Fig. 4, the MMIC LNA consists of two stages. In the LNA design, the FET must be biased at high gain and low noise operation region, so that the optimum bias point was chosen at \(V_{ds}\) of 2V and \(V_{gs}\) of -0.6V in this circuit.

The first stage of this circuit was mainly designed for minimum noise figure, while the second stage is fully for achieving maximum gain. A degeneration inductance \(T4\) is connected directly to the source of \(M_1\), and this inductance can adjust the noise impedance matching of \(M_1\). By selecting a suitable \(T2\), the real part of the input impedance of \(M_1\) will tend toward 50Ω. Therefore, an input matching network can be constructed to achieve minimum noise figure and gain matching simultaneously. A shunt-shunt (R1-C3) feedback was applied to stabilize the low frequency K factor [1].

Fig. 5 shows the S-parameters measured results of the Ka-band LNA. The small signal gain has a peak of 12.53 dB at 30GHz with 3-dB bandwidth of 5.3 GHz from 27.3GHz to 32.6GHz. The input return loss is greater than 10dB with a maximum value of 16.66dB at 34GHz, and output return loss is greater than 7.57 dB at 30GHz. The noise figures were measured below 26.5GHz. And the minimum noise figure of 3.8dB was found at 30GHz.

The circuit schematic and die photo of wideband PA was shown in Fig.6 and this is cascade architecture. R1 and C were used for minimize the low frequency oscillation at high power operation [2]. The total DC
power consumption of this amplifier was 780 mW, which included \( I_{DS} \) of 66 mA and \( V_{DS} \) of 4 V in the driver stage (gate width = 2 fingers x 100 \( \mu \)m), and \( I_{DS} \) of 129 mA and \( V_{DS} \) of 4V in the output power stage (gate width = 4 fingers x 100 \( \mu \)m). Fig. 6 illustrates the signal gain (\( S_{21} \)) of 5 dB, the input return loss (\( S_{11} \)) of -18 dB and output return loss (\( S_{22} \)) of -9.5 dB at 30 GHz, respectively. The wideband PA exhibited the highest \( S_{21} \) at 12 GHz.

In the power measurement, the Fig. 7 depicts the on-wafer measured output power, gain and PAE at \( V_{DS} = 4 \) V, \( I_{DS} = 209 \) mA and 12 GHz. The \( P_{1dB} \) was attained with about 18.6 dBm, the saturation output power was achieved with 21 dBm, and the maximum PAE was obtained to 18.3 % at \( P_{in} = 8 \) dBm.

Furthermore, it should be interesting to note the third intercept inter-modulation (\( I_{IP3} \)), which could describe specificity index of circuit dynamic range. In other words, the input signal is fed to two tones in the amplifier, and it will produce the fundamental power and high order harmonic power inter-modulation products. Hence, two-tone evaluation was performed at frequencies of 12 GHz and 12.001GHz, which were mixed to produce inter-modulation products in the power amplifier. The \( I_{IP3} \) of 1.4 dBm and the \( O_{IP3} \) of 24.5 dBm were achieved.

The singly balanced mixer utilizes as the mixing architecture in this work. The Schottky diode (connected device drain and source terminal) were zero biased, since they had very good non-linearity at this condition. The simulation results were derived from harmonics balanced simulation using ADS, Momentum, and EEHET model supported by WIN™. As for the IF filter, it is realized by the lumped elements and it is centered at 1 GHz. The design schematic and die photo of single balanced mixer were show in figure 8. The chip size is 1×0.6 mm².

Fig. 6 The circuit schematic and die photo of wideband PA

Fig. 7 The power measurement of wideband PA at 12 GHz

Fig. 8 The circuit schematic and die photo of SB mixer

Fig. 9 shows the simulated and measured performance by on wafer probing. The mixer has conversion loss of -7 dB at 30GHz at 29 GHz with LO drives at 10 dBm. The simply architecture and good performance are beneficial for using at up and down converter system. Moreover, low power consumption is also an advantage of this circuit.

Fig. 9 The simulated and measured conversion loss of mixer
The design schematic and die photo of L-C feedback voltage controlled oscillator were shown in Fig. 10. The VCOs, if monolithically integrated with the power amplifiers, can provide flexible high-power signal sources for a broader range of applications [3]. In the design of VCO, the measured small-signal parameters used for checking VCO oscillation frequency and EEHEMT large-signal model was used to simulate oscillator output power and phase noise. The L2 and C3 were series connected between M1 gate and drain terminals, providing a positive feedback to make the HEMT more unstable. The lump elements nearby M1 were adjusted to make the S11 output of smith chart at expected frequency and generated a negative resistance. The negative resistance should be 3 times larger than the positive resistance provided by resonant tank. M2 was operated as a varactor and no dc power consumption was found due to the dc path of M2 was series to C7.

The HEMT’s gate and drain bias points were set to -1 and 2 V (Ids=15 mA), respectively, which was experimentally found to be optimal for both phase noise and the tuning frequency range. A typical output power spectrum is shown in Fig. 11 at a tuning voltage of 2 V. The output power at the resonance frequency (23.1 GHz) is -5 dBm. The dc power consumption of this VCO is 30 mW. The phase noise is less than -96 dBc/Hz at 1 MHz offset within the entire tuning range. To evaluate the overall performance of the VCO, a common figure of merit (FOM) is used and this value is around -165 dBc/Hz.

CONCLUSIONS

The Ka-band millimeter wave monolithic ICs using WIN 0.15μm power pHEMT (PP15-20) were investigated and demonstrated in the study. According to the measured experimentally results, the all of ICs with CPW microstrip line interconnection exhibited good performance. Therefore, expensive back-side process was avoided in this technology. The CPW mode millimeter wave ICs and modules can be highly integrated due to its low cost and high performance[4].

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References