Device Performance of AlGaN/GaN MOS-HEMTs Using La$_2$O$_3$ high-k Oxide Gate Insulator

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Abstract

AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs) using La$_2$O$_3$ as gate oxide by electron-beam evaporated have been investigated and compared with the regular HEMTs [1]. The La$_2$O$_3$ thin film achieved a good thermal stability after 200°C, 400°C and 600°C post-deposition annealing due to its high binding energy (835.7 eV) characteristics. Our measurements have shown that La$_2$O$_3$ MOS-HEMTs exhibiting the best characteristics, including the lowest gate leakage current, the largest gate voltage swing, and pulsed-mode operation. In addition, a negligible hysteresis voltage shift in the C-V curve can be improved significantly after high temperatures annealing.

1. Introduction

Many investigations of GaN field-effect transistors (FETs) and AlGaN/GaN heterostructure FETs (HFETs) have reported excellent device breakdown voltage and high thermal stability due to its wide bandgap property [2-3]. AlGaN/GaN HFETs are treated as the best candidate material for high-power microwave devices and DC-DC converter applications [4]. However, the gate leakage current of the AlGaN/GaN HFET is typically as high as 10-100 μA/mm at room temperatures, and increase almost three orders in magnitude at 750°C that will limit the applications of industry [5]. Moreover, AlGaN/GaN HEMTs also exhibit current collapse and capacitance-voltage (C-V) hysteresis phenomena under a high input power swing operation [6-7]. These characteristics resulted in the output power density degradation and undesired harmonic signals generation. By inserting a high dielectric constant (high-k) insulating materials such as SiN$_x$, Pr$_2$O$_3$, Gd$_2$O$_3$, Ga$_2$O$_3$, plasma enhance chemical vapor deposition (PECVD) SiO$_2$, sputtered-HfO$_2$, sputtered-Sc$_2$O$_3$ and others were involved of GaN-based MOS-HEMTs. However, the plasma induced surface damage on AlGaN Schottky layer still can not be avoided for these sputtered- or plasma-enhanced high-k insulator depositions. Furthermore, the gate metal was deposited using electron-beam evaporator after leaving the high-k material growth environment; therefore, the fix charge between metal–oxide interfaces still exists and became an additional problem. Besides these, the complicate gate formation procedure of the mentioned technologies is also difficult for high volume industry production. In this study, samples of rare-earth lanthanum were electron-beam evaporated with an oxygen flow rate to form the high quality high-k oxide layer, and then in-situ Ni/Au metal were deposited in the same high vacuum chamber. The dielectric constant of La$_2$O$_3$ insulator developed in this study is 10.4. By using C-V curves, the voltage shift of C-V hysteresis phenomena can be reduced to 0.04 V after 800°C post annealing. The proposed La$_2$O$_3$/AlGaN/GaN MOS-HEMTs were indicated to have high-frequency and high-breakdown capabilities.

2. Lanthanum Oxide Growth and Wafer Preparation

The schematic cross section of a La$_2$O$_3$/AlGaN/GaN MOS-HEMTs used for this study is shown in Fig. 1. Before the demonstration of La$_2$O$_3$/AlGaN/GaN MOS-HEMTs, the optimization of electron-beam evaporated La$_2$O$_3$ high-k thin film should be carried out by adjusting the oxygen flow rate in the chamber, which a 10 nm thick, rare-earth metal (La) was initially evaporated with an oxygen flow rate between conventional Ni/Au gate and AlGaN to reduce the gate leakage current. The AlGaN/GaN HEMT heterostructures in this study were grown by atmospheric pressure metal organic chemical vapor deposition (AP-MOCVD) on 2 in. sapphire wafers. The 4000
nm undoped GaN was first grown for buffer and channel layers. Then a 30 nm undoped Al_{0.30}Ga_{0.70}N layer was grown for Schottky layer. The designed structure demonstrated a sheet charge density of $1.685 \times 10^{13}$ cm$^{-2}$ together with a Hall mobility of 983 cm$^2$/V·sec at 300 K. For device fabrication, the active region was protected by photo-resist and mesa isolation region was removed by BCl$_3$ + Cl$_2$ mixture gas plasma in reactive ion etcher (RIE) chamber [6]. The ohmic contacts of Ti/Al/Ni/Au (25nm/125nm/50nm/100nm) metals were deposited by electron-beam evaporation and patterned by a conventional optical lithography and lift-off technology followed by 850 °C, 30 s RTA annealing in N$_2$ ambient. Then, a 10 nm thick praseodymium was first evaporated with an optimal oxygen flow rate. During this stage, the chamber pressure will increase to around 10$^{-4}$ torr. After the chamber pressure was reduced to 3 × 10$^{-7}$ torr, the conventional Ni/Au (30nm/150nm) gate metals were deposited. For comparison, the traditional Ni/Au Schottky gate GaN HEMT was also fabricated. Finally, the Ti/Au (30nm/150nm) metals were deposited for interconnection and probe pads, and a 200nm SiO$_2$ was deposited for device passivation.

3. Experimental Results and Discussion

Fig. 2 shows the XPS 3d core level spectra of La$_2$O$_3$ at various temperatures. It showed that the binding energies of our developed La$_2$O$_3$ after 200°C, 400°C and 600°C post-annealing were closed to the standard value, 836 eV in 3d core level, which is recorded in handbook of x-ray photoelectron spectroscopy. It also showed the high signal intensities of La$_2$O$_3$. Therefore, it concluded that a high quality and a high thermal stability high-k insulator can be obtained by using electron-beam evaporated La with an oxygen flow rate.

The capacitance-voltage (C-V) measurements and hysteresis voltage shift versus various temperatures were shown in Fig. 3, which were performed at 1 MHz on MOS-ring capacitors with a diameter of 100 µm. The sharp transition from two dimensional electron gas (2-DEG) accumulation to depletion demonstrates few pinning phenomenon of the Fermi-level at the AlGaN/La$_2$O$_3$ interface and resulting in a high quality interface. A charge-injection-type hysteresis voltage shift of 0.16 V is observed in the C-V loop measurement after 200°C post annealing and this value can be improved to 0.04 V after 800°C post annealing. Moreover, using the observed accumulation capacitance, the dielectric constant of La$_2$O$_3$ is estimated to be 10.4. On the other hand, an increase in the capacitance was observed at gate biases beyond +2 V. This is due to a charge spillover from the 2DEG channel, which brings some of the carriers closer to the surface, thus decreasing the barrier layer effective thickness and increasing the capacitance.
4. Device Characteristic Comparisons

The gate-to-drain voltage dependences of the gate leakage currents for standard GaN HEMTs and La$_2$O$_3$ MOS-HEMTs were shown in Fig. 4. From the figure, the MOS-HEMTs design demonstrated more than one order of magnitude lower gate leakage compared to that of the standard HEMTs. The lower gate leakage current not only improves the device breakdown voltage but is also beneficial to the improvement of the power-added-efficiency (PAE) at high input power swing. Fig. 5 and Fig. 6 show the transistor $I_{ds}$-$V_{ds}$ characteristics, and $V_{gs}$ dependence of transconductance ($g_m$) and $I_{ds}$ curves at a fixed $V_{ds}=8$ V for two devices, respectively. The maximum drain-to-source current ($I_{dmax}$) and peak transconductance were 652.9 mA/mm and 572.7 mA/mm for standard HEMTs and La$_2$O$_3$ MOS-HEMTs, respectively. The maximum transconductance ($g_m$) biased at $V_{ds} = 8$ V for standard HEMTS and La$_2$O$_3$ MOS-HEMTs were 88.8 mS/mm and 59.4 mS/mm, respectively. Because of the MOS-HEMTs architecture, the gate-to-channel control ability was suppressed due to a high-k insulator was inserted, and then caused an effective modulation distance of depletion region increasing between metal gate and channel. Therefore, standard HEMTs obtained higher drain-to-source current and peak $g_m$ than La$_2$O$_3$ MOS-HEMTs.

Pulse measurements of electronic devices are used popularly to characterize their trapping phenomena and device heating effects. The response time of these trapping carriers dominates the performance of pulse measurement. The response times of these trapping carriers are typically of the order of $\mu$s, which are much longer than the ns times of electron carrier transportation, especially in high-speed and high-power devices. Fig. 7 shows the pulse I-V measurements with various pulse periods for $1 \times 100$ $\mu$m$^2$ devices at $V_{gs}$ of 0 V and $V_{ds}$ of 8 V for both devices. The surface state related dispersion effect causes the current density at high current to decay by reducing the pulse width. As shown in figure, the standard GaN HEMTs show a larger slope versus pulse period compared to La$_2$O$_3$ MOS-HEMTs. Moreover, low-frequency noise measurement were conducted to elucidate further the relationship between the flicker noise and gate electro-interface; the measurement scheme was sensitive to the
Table I. The dc and rf characteristic comparisons of standard HEMT and \(\text{La}_2\text{O}_3\) MOS-HEMT.

<table>
<thead>
<tr>
<th>Measurement results</th>
<th>(V_{\text{ON}})</th>
<th>(V_{\text{BK}})</th>
<th>(V_p)</th>
<th>(I_{\text{dmax}})</th>
<th>Peak (g_m)</th>
<th>(f_\Gamma)</th>
<th>(f_{\text{max}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN HEMT</td>
<td>1.04V</td>
<td>-117.95V</td>
<td>-7V</td>
<td>652.9 mA/mm</td>
<td>88.8 mS/mm</td>
<td>6.9 GHz</td>
<td>11.6 GHz</td>
</tr>
<tr>
<td>(\text{La}_2\text{O}_3) MOS-HEMT</td>
<td>1.49V</td>
<td>-131.30V</td>
<td>-8.5V</td>
<td>572.7 mA/mm</td>
<td>59.4 mS/mm</td>
<td>6.3 GHz</td>
<td>10.7 GHz</td>
</tr>
</tbody>
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Fig. 8 Flicker noise spectra of both devices.

semiconductor surface. The bias used in low-frequency noise measurement is \(V_{gs} = 8\) V associated with an \(I_d\) of 100 mA/mm for both devices. As shown in Fig. 8, the \(\text{La}_2\text{O}_3\) MOS-HEMTs performed a lower 1/f noise obviously spectra improvement compared to standard HEMTs. It indicated that lower surface states can be achieved with this electron-beam evaporated high-k \(\text{La}_2\text{O}_3\) film and the conventional plasma induced surface states can be avoided. In consequence, the \(\text{La}_2\text{O}_3/\text{AlGaN}\) interface with 800°C post-annealing achieved a lower surface density than traditional Ni/Au/AlGaN interface.

5. Conclusion

In conclusion, improvement \(\text{La}_2\text{O}_3\) MOS-HEMTs demonstrate a lower gate leakage currents, and a better interface between high-k insulator oxide layer and AlGaN substrate in this study. By using electron-beam evaporated Lanthanum oxide layer at an oxygen flow rate environment, the MOS-gate architecture can be realized in the same chamber which is beneficial for industry high-volume production. Besides, the plasma-induced surface states can be avoided simultaneously compared to sputtered- or plasma-enhanced deposition high-k insulators. The improvement of \(\text{La}_2\text{O}_3\) MOS-HEMTs is primarily due to the quenching of GaN surface states, which would otherwise trap electrons and cause device performance degradation. Moreover, the charge-injection-type hysteresis voltage shift of 0.16 V is observed in the C–V loop measurement after 200°C post annealing and this value can be minimized to 0.04 V after 800°C post annealing. Based on the dc measurement, pulse measurement, flicker noise measurement, the results concluded that low surface state and low gate leakage current \(\text{La}_2\text{O}_3\) MOS-HEMTs exhibit a better interface between \(\text{La}_2\text{O}_3\) and AlGaN, and high-temperature applications.

6. References


